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Multi sampled Multilevel Inverters to Improve Control Performance

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ABSTRACT

This paper presents The multisampling technique which is developed to reduce switching delay. However, the control gains are still limited by the switching frequency. To demonstrate an alternative way of improving the control performance without increasing the switching frequency, this paper discusses multisampled multilevel inverters. The example of a voltage controlled multilevel inverter with cascaded control loops is provided. The proposed method also is used to minimize the Total Harmonic Distortion THD of the synthesized multilevel waveform. A comparison between symmetric and asymmetric MLI using variable frequency carrier based pulse width modulation technique is done. The proposed modulation technique eliminates the problem of unbalanced switch utilization resulting in reduced total harmonic distortion and reduced switching losses. The proposed system was verified through simulation and Hardware.

Index Terms—Multisampled multilevel inverter, pulse modulated (PWM), Total harmonic distortion (THD).

1.INTRODUCTION

MULTILEVELvoltage-source inverters are a suitable configuration to reach high power ratings and high quality output waveforms besides reasonable dynamic responses. Among the different topologies for multilevel converters, the cascaded multilevel inverter has received special attention due to its modularity and simplicity of control. The principle of operation of this inverter is usually based on synthesizing the desired output voltage waveform from several steps of voltage, which is typically obtained dc voltage sources. To control the output voltage and toeliminate the undesired harmonics in multilevel converters with equal dc voltages, various modulation methods such as sinusoidal pulse width modulation (PWM) and space-vector PWM techniques are suggested.

However, PWM techniques are not able to eliminatelower order harmonics completely. Another approach is to choose the switching angles so that specific higher order harmonics such as the 5th, 7th, 9th, are suppressed in the output voltage of the inverter. This method is known as selective harmonic elimination (SHE) or programmed PWM techniques in technical literature. A fundamental issue associated with such method is to obtain the arithmetic solution of nonlinear transcendental equations which contain trigonometric terms and naturally present multiple solutions. This set of nonlinear equations can be solved by iterativetechniques such as the Newton–Raphson method.However, such techniques need a good initial guess which should be very close to the exact solution patterns. Furthermore, this method finds only one set of solutions depending on the initial guess. Therefore, the Newton–Raphson method is not feasible to solve the SHE problem for a large number of switching angles if good initial guesses are not available.

A systematic approach to solve the SHE problem based on the mathematical theory of resultant is proposed , where transcendental equations that describe the SHE problem are converted into an equivalent set of polynomial equations and then the mathematical theory of resultant is utilized to find all possible sets of solutions for this equivalent problem.

This method is also applied to multilevel inverters with unequal dc sources. However, applying the inequality of dc sources results to the asymmetry of the transcendental equation set to be solved and requires the solution of a set of high-degree equations, which is beyond the capability of contemporary computer algebra software tools.

This paper compares three different topologies of inverters The multilevel inverters are 5-level,7-level and 9-level inverters. This comparison is done with respect of power losses, cost, weight and THD. The switching pattern for inverters is explained as well. For each inverter, IGBTs and MOSFETs are used as switching devices to make the comparisons more accurate. The

switchesthat are used for different inverters are the same for all of the inverters.

If the THD is important, the 9-level inverters should be used, since it has a lower THD than the 7-level and the 5-level inverter. The 9-level multilevel inverters have the lowest THD when filters are not used. Their THD is about 4.87%. To select a multilevel inverter is a tradeoff between cost, complexity, losses and THD. The most important part is to decide which one is more important.

II. STRUCTURE OF THE SYMMETRICAL 5-LEVEL MULTILEVEL INVERTER

Multilevel inverters are promising, they have nearly sinusoidal output voltage waveforms, output current with better harmonic profile, less stressing of electronic components owing to decreased voltages, switching losses that are lower than those of conventional two level inverters, a smaller filter size, and lower EMI, all of which make them cheaper, lighter, and more compact. Various topologies for multilevel inverter have been proposed over the years. Common one is diode clamped, flying capacitor, cascaded H-bridge and modified H-bridge multilevel. This paper recounts the development of a nine level inverter.

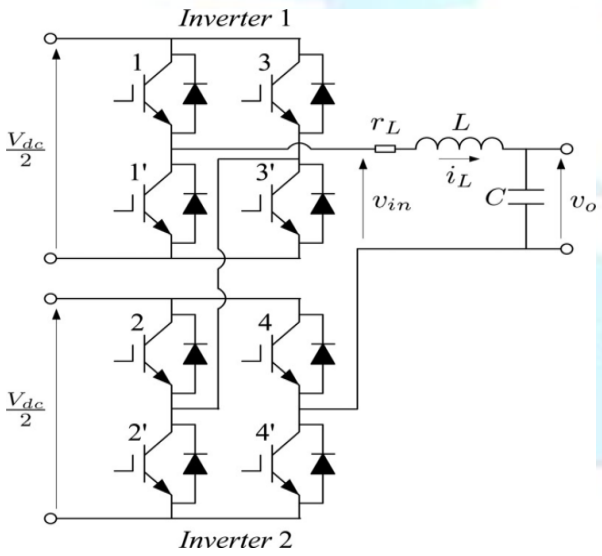

Figure 1

Symmetrical 5 Level Multilevel inverter

The control performance provides a detailed analysis of the symmetrical 5 level system operation. The system comprises of two cascaded H-bridges inverters and modulated by four phase-shifted triangle carriers with coupled –sampling frequency is modeled.In order to get the better performance and better output. We are going for the asymmetrical multilevel inverter .

III.PROPOSEDMULTILEVELINVERTER TOPOLOGY

The proposed system is capable of producing Nine level of output which can be connected to the grid. It comprises a single phase inverter, three diodes, and seven switches shown in Fig.1. The modified inverter topology is significantly advantageous over other topologies i.e. less power switches, power diodes, and no capacitors used for the same inverters of the same number of levels.

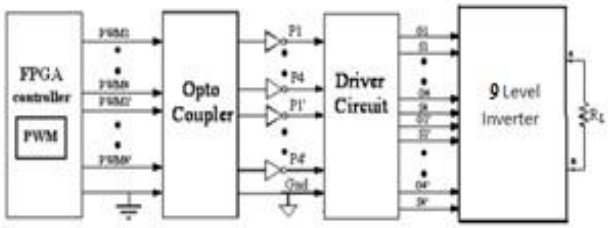

Figure 2

Basic Block Diagram of Asymmetrical multilevel inverter

The above diagram shows the basic structure of the asymmetrical 9 level multilevel inverter.

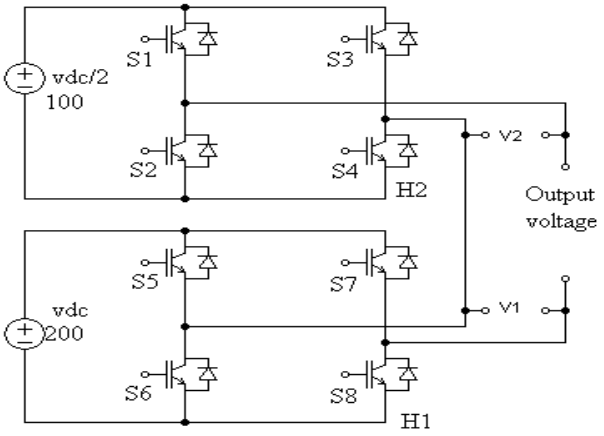

Figure 3

Asymmetrical 9 Level Multilevel inverter

In order to get the better performance and better output. We are going for the asymmetrical multilevel inverter .
In the Fig 3 it is clearly shown that the input given to the system is the variable DC source hence the system is called as Asymmetrical multi level inverter.

IV.FUNCTIONAL BLOCK DIAGRAM OF FPGA

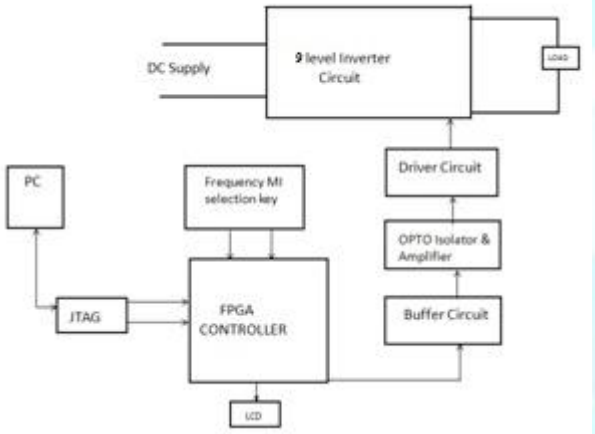

Figure 4

An FPGA is a regular structure of logic cells or modules and interconnect which is under the designer's complete control. This means the user can design, program and make changes to his circuit whenever he wants.

Field Programmable Gate Arrays (FPGAs), as the name suggests these devices are a uniform array of gates that can be updated by the designer on the board as and when required. In some cases these devices are known as ASICs (Application Specific Integrated Circuits), that is each device is configured by the designer to perform a function particular to his application. In most ASIC technologies, gate level interconnections areestablished when the device is manufactured (i.e. custom and semi-custom ASICs).

FPGA Advantage

1. Enhanced flexibility
2. Reduced board space, power and cost
3. Increased performance

All FPGAs have the following key elements:

The Programming technology, basic logic cells, I/O logic cells, Programmable interconnect, Software to design and program the FPGA

SPARTAN-3 EFPGA: The Spartan™-3E family of Field-Programmable Gate Arrays (FPGAs) is specifically designed to meet the needs of high volume, cost-sensitive consumer electronic applications. The five-member family offers densities ranging from 100,000 to 1.6 million system gates, as shown in Table. The Spartan-3E family builds on the success of the earlier Spartan-3 family by increasing the amount of logic per I/O, significantly reducing the cost per logic cell. New features improve system performance and reduce the cost of configuration. These Spartan-3E enhancements, combined with advanced 90 nm process technology, deliver more functionality and bandwidth per dollar than was previously possible, setting new standards in the programmable logic industry. Because of their exceptionally low cost, Spartan-3E FPGAs are ideally suited to a wide range of consumer electronics applications, including broadband access, homenetworking, display/projection, and digital television equipment. The Spartan-3E family is a superior alternative to mask programmed Asics. FPGAs avoid the high initial cost, the lengthy development cycles, and the inherent inflexibility of conventional ASICs. Also, FPGA programmability permits design upgrades inthe field with no hardware replacement necessary, impossibility with ASICs.

Opto coupler

The function of an Opto isolator is to isolate the control circuit from the power Circuit. The name of this opto coupler IC is 6N137.

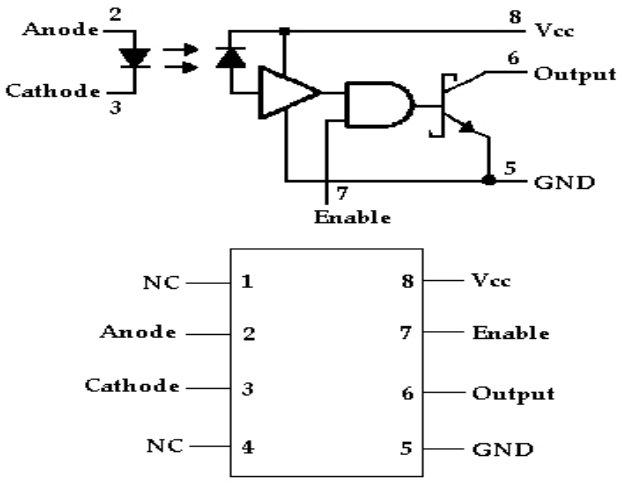

Figure 5

Gate driver

Gate driver acts as high power buffer stage between the PWM control device and gates of the primary power switching Devices likes as MOSFET, IGBT.

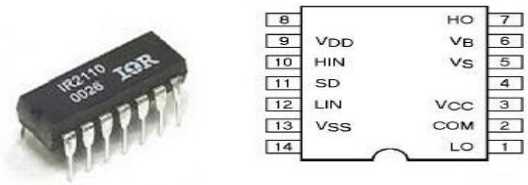

Figure 6

V.PULSEWIDTH MODULATION

A PWM waveform is a sequence of pulses with fixed frequency but varying pulse widths. The width of the pulse might vary from 0% to 100% of the fixed period.

1. Types of PWM
2. Single PWM
3. Multiple PWM
4. Sine PWM
5. Space Vector PWM

The diagram shows how comparing a ramping waveform with a DC level produces the PWM waveform that we require. The DC signal can range between the minimum and maximum voltages wave of the triangle.

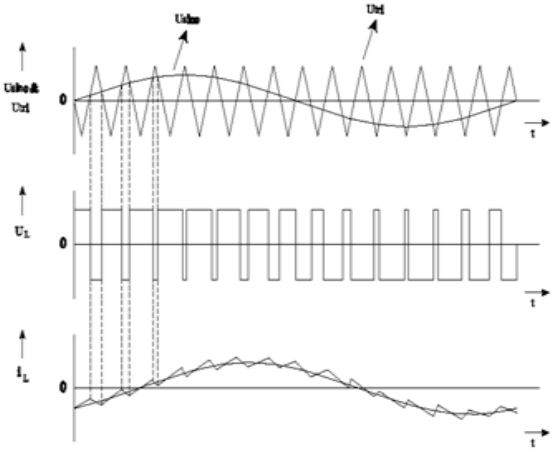

Figure 7

When the triangle waveform voltage is greater than the DC level, the output of the op-amp swings high, and when it is lower, the output swings low. The sinusoidal waveform is compare to the Carrier (Triangular wave) signal; the Comparator output PWM is called SPWM.

VI.SIMULATION DIAGRAM FOR PROPOSED SYSTEM

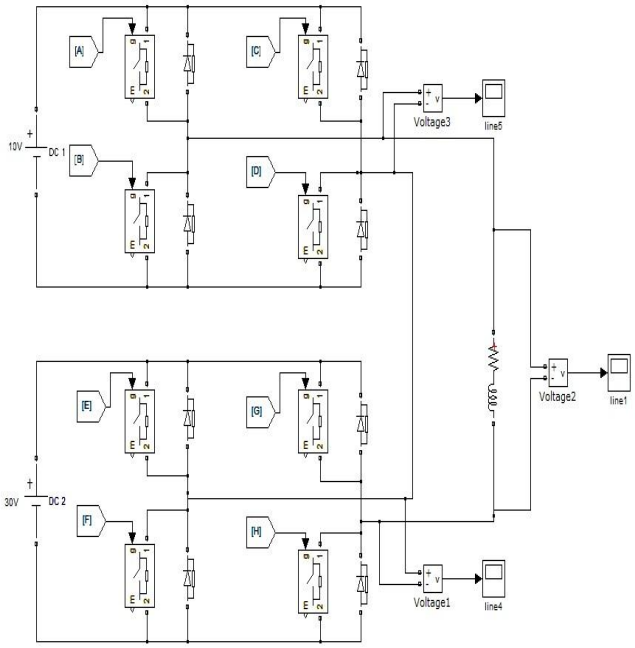

Figure 8

The figure 8 shows the simulation diagram of proposed asymmetric multilevel inverter

Comparison Between Asymmetric Inputs 5 level, 7 level and 9 level cascaded MLI

Topology	5 Level Inverter	7 Level Inverter	9 Level Inverter
Fundamental Frequency	20.04	29.99	40.02
Total Harmonic Distorsion	9.92%	6.55%	4.88%

VII.FFT AND THD VALUES

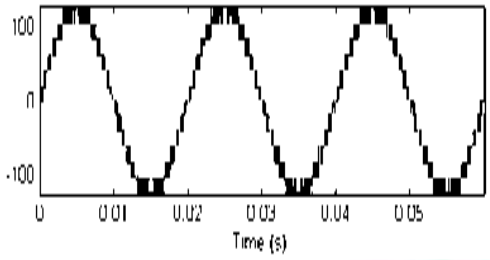

Figure 9

Fundamental frequency(50 Hz)=40.02 and
THD=4.88%

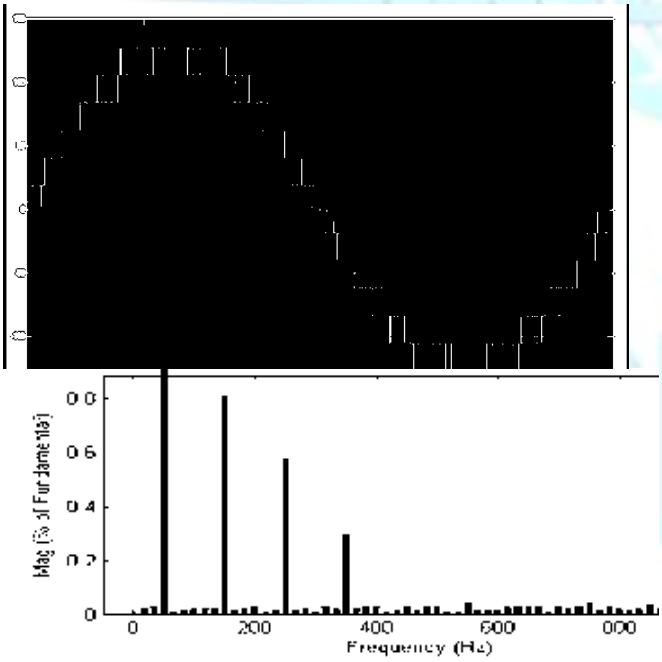

Figure 10

The THD result of the output line voltage shown in Fig.9 which is calculated according to the following, is 4.88%:

$$THD = \sqrt{\sum_{n=5,7,11,\ldots}^{49} V_n^2} \Big/ V_1.$$

VIII.SIMULATION RESULTS

To validate the computational results for switching angles, a simulation is carried out in MATLAB/SIMULINK software for an 9-level cascaded H-bridge inverter and unequal dc sources.

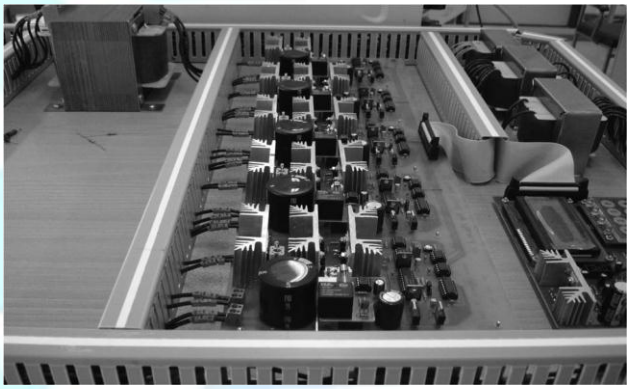

Figure 12

Implemented 9-level cascade H-bridge prototype.

IX. CONCLUTION

In this paper, I have dealt about the proposed asymmetric 9-level multilevel inverter, since there are less number of power switches as a result of which the switching losses are reduced and THD value obtained is 4.8%. As a result of which it gives a better performance with limited resource utilization.

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